REMARKS

Claims 1, 3, 4, 6, 7, and 9 have been examined, with all claims remaining rejected.

Specification; and Claim Rejections – 35 U.S.C. 112, First Paragraph

The specification has been objected to as failing to provide proper antecedent basis for adjusting the clock frequency non-incrementally. Also, claims 1, 3, 4, 6, 7, and 9 have been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description and enablement requirements; it is the Examiner's position that the specification does not explicitly teach adjusting the clock frequency non-incrementally.

Applicant respectfully disagrees. One of ordinary skill in the art reading the application as a whole understands that the application as originally filed describes a clock frequency that is adjusted non-incrementally.

The application describes a frequency regulating circuit that compares an instantaneous current consumption with a threshold value. If the instantaneous current consumption is lower than the threshold value, individual clock pulses pass through, and if the instantaneous current consumption is higher, the individual clock pulses are suppressed. The frequency regulating circuit adjusts the clock frequency immediately.

The application does not describe an incremental reduction/increase in clock frequency. For example, the application does not describe skipping 1 out of 4 clock pulses, then 2 out of 4 clock pulses, then 3 out of 4 clock pulses, as illustrated in Durham in Figures 2, 3, or 4, or as described in column 3, line 50, through column 4, line 16. The application does not describe or suggest a state machine for switching between different levels. The clock frequency therefore must be adjusted non-incrementally.

Reconsideration and withdrawal of this objection and rejections are therefore respectfully requested.

Drawings

The drawings are objected to for allegedly not showing adjusting the clock frequency non-incrementally.

The non-incremental feature is not a structural detail, and therefore illustrating it in the drawings is not essential for a proper understanding of the disclosure. This feature therefore need not be shown in the drawings. However, Figure 2 illustrates that the individual clock pulses output from the filter are suppressed, and thus the clock frequency is adjusted non-incrementally. It is not clear to Applicant how the Examiner would expect such a feature to otherwise be shown.

Reconsideration and withdrawal of this objection are therefore respectfully requested.

Claim Rejections – 35 U.S.C. 112, Second Paragraph

Claims 1, 3, 4, 6, 7, and 9 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. It is the Examiner's position that the term "non-incrementally" is indefinite.

Applicant respectfully disagrees. "Incrementally" is well known to mean something performed in a series of regular additions or contributions, and thus "non-incrementally" must mean something performed that is not in a series of regular additions or contributions. Therefore, adjusting a clock frequency instantaneously and non-incrementally must mean that the clock frequency is adjusted instantaneously in a single step. The term "non-incrementally" is therefore not indefinite.

Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections – 35 U.S.C. 103

Claims 1, 3, 4, 6, 7, and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Durham et al. (US 5,761,517; hereinafter "Durham") in view of Wang (US 5,943,203).

Applicant respectfully traverses this rejection.

Independent claim 1 recites "A frequency regulating circuit ... comprising ... a pulse filter ... configured to suppress at least one clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that said control device adjusts said clock frequency instantaneously and non-incrementally to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit."

The clock pulse is suppressed in response to the control signal such that the control device adjusts the clock frequency instantaneously and non-incrementally, and therefore the frequency regulating circuit of independent claim 1 has a fast reaction time. As soon as current consumption exceeds a predefined threshold value, at least one clock pulse is suppressed. During this suppression there is no longer a load. A brief time later the current consumption falls below the threshold value, and the clock pulse suppression is stopped. This process can be repeated again and again depending on the current profile. There is only full frequency mode (i.e., no clock pulse suppression) or no frequency mode (i.e., clock pulse suppression), and nothing in between (e.g., 3 clock pulses passed, 5 suppressed, 2 passed, 3 suppressed, etc.).

In contrast, Durham's circuit has the clock frequency is adjusted incrementally.

Referring to Durham's Figures 1A and 1B, Durham's circuit changes the output of an oscillator clock 27 prior to its input to dynamic logic circuit elements as a system clock signal 20. The oscillator clock signal is controlled based upon a signal generated by a sensor 18 that determines the power consumption of the integrated circuit. The frequency of the clocked signal 20 is reduced/increased incrementally (explained below) based upon the determined level of power consumption. A pattern generator 17 inputs a digital signal to a series of interconnected registers 10, 11, 12, 13 which make up a loadable shift register. The output of the pattern generator 17 is based upon the input from the sensor 18. The bits shifted through the shift register are ANDed 7 with the oscillator clock signal to control the frequency of the system clock 20. Durham's

frequency levels are therefore not adjusted directly in response to a control signal, as required by independent claim 1.

Regarding the incremental reduction/increase of frequency, Durham has defined frequency levels 4, 3, 2, 1, 0. See Durham, Figure. 2. Level 4 represents the speed of the system clock 20 equaling the speed of the oscillator clock 27. Level 3 represents the speed of the system clock 20 being 75% of the speed of the oscillator clock 27, that is 3/4 clock pulses passing. Level 2 represents the speed of the system clock 20 being 50%, that is 2/4 clock pulses passing. Level 1 represents the speed of the system clock 20 being 25%, that is 1/4 clock pulses passing. Level 0 represents no clock pulses passing, that is when the system is turned off. See Durham, Figure 4. This frequency increase/decrease happens incrementally using the shift register shown in Figures 1A and 1B and described above. As illustrated in Figure 4, the frequency levels can not be changed from level 4 to level 1 instantaneously. The frequency level increase/decrease happens gradually, making Durham's reaction time significantly slower than that of the circuit of independent claim 1. Durham therefore does not disclose adjusting the clock frequency instantaneously and non-incrementally, as required by independent claim 1.

Wang fails to make up for Durham's deficiencies.

Independent claim 1 is therefore patentable over the applied references for at least these reasons.

Since independent claims 4 and 7 include limitations similar to the limitations discussed above with respect to independent claim 1, they are patentable over the applied references for at least the same reasons.

All other claims depend either directly or indirectly from the independent claims, and are therefore patentable over the applied reference for at least the same reasons.

Reconsideration and withdrawal of the prior art rejection are therefore respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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